(b) depositing oxide films in the grooves by a CVD method using a non doped organic silicon source;

(c) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(d) annealing the oxide films, after said removing, at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}.

10. (Twice amended) The method of claim 9, wherein the CVD method is any of atmospheric pressure CVD method, low pressure CVD method, plasma CVD method, photo CVD method, and liquid phase CVD method.

25. (Thrice amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate, each of grooves having a width narrower than 0.5μm;

(b) depositing oxide films in the grooves by a CVD method using a non doped organic silicon source;

(c) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so the dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than 1 μm^{-2}; and

(d) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate serving as a

top surface of a corresponding device region.

26. (Thrice amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate, each of grooves having a width narrower than 0.5μm;

(b) burying oxide films in the grooves by a CVD method using a non doped organic silicon source; and

(c) annealing said oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, and an etching rate by ammonium fluoride solution of said oxide films is less than 130 nm/min, which is substantially identical to that of a thermal oxide film.

27. (Thrice amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate, each of grooves having a width narrower than 0.5μm;

(b) burying oxide films in the grooves by a CVD method using a non doped organic silicon source; and

(c) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C, but less than or equal to 1350°C so that said oxide films include higher order ring structures higher than 5-fold ring and lower order ring structures lower than 4-fold ring at respective predetermined rates, the respective predetermined rates of the ring structures are determined according to rates of integrated Raman intensities corresponding to respective

ring structures to a total integrated Raman intensity, and the structures are formed to satisfy either of or both conditions that said higher order ring structures are substantially more than 85 % of an overall structure and said lower order ring structures are substantially less than 15 % of the overall structure.

28. (Thrice amended) A method of manufacturing a semiconductor substrate having shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by a CVD method using a non doped organic silicon source;

(d) removing upper parts of the oxide films so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region; and

(e) annealing the oxide films, after said removing, at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the corresponding device region in a vicinity of the grooves is less than 1 μm^{-2}.

29. (Thrice amended) A method of manufacturing a semiconductor substrate having a shallow trench isolation regions and device regions sandwiched by the shallow trench isolation regions, comprising:

(a) forming a plurality of grooves on part of a surface of the semiconductor substrate;

(b) forming thin thermal oxidation films on the inner walls of the grooves;

(c) depositing oxide films directly on the thin thermal oxidation films by a CVD

method using a non doped organic silicon source;

(d) annealing the oxide films at a substrate temperature which is greater than or equal to 1150°C but less than or equal to 1350°C so that dislocation density generated in the semiconductor substrate in a vicinity of the grooves is less than 1 μm^{-2}; and

(e) removing upper parts of the oxide films, after said annealing, so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed, each of the exposed surface areas of the semiconductor substrate serving as a top surface of a corresponding device region.

36. (Amended) A method for forming a microelectronic structure, the method comprising:

(a) forming a mask layer on a substrate wherein the mask layer exposes a part of the substrate;

(b) forming a groove in the exposed part of the substrate

(c) depositing a layer of an insulating film using a non doped source so as to fill the groove and cover the mask layer;

(d) annealing said insulating film at a temperature which is greater than or equal to 1150°C but less than or equal to 1350°C.

45. (Amended) The method of claim 44, wherein said depositing the insulating material comprises forming an oxide by a CVD method using the non doped source.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 9-11, 14-46, and 48-53 are pending in this application. Claims 16-23 have been withdrawn from consideration. Claim 47 has been canceled without prejudice or